Timing Compensation for an Excimer Laser Solid-State Pulsed Power Module (SSPPM)

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***Abstract*—For certain applications, it is critical to minimize variations in the (throughput) timing between trigger and the output pulse of a magnetic modulator. A circuit is described in this paper that maintains a relatively constant delay over a large operating voltage range (600–1150 V) and temperature range (25 °C–65 °C) range. The circuit operates by sampling the charging voltage and magnetic switch temperature just prior to the start switch trigger. Those parameters are then used to calculate the appropriate amount of delay to add into the low-level trigger chain to ensure that the delay stays constant over the voltage and temperature operating range. Although other approaches can be conceived and implemented, this particular design is relatively simple and inexpensive and meets the desired performance goals. Data presented show that the ideal correction function is nonlinear in nature and, as a result, simple linear approximations are limited in their ability to minimize the timing variations. Improvements to the original circuit use a multiple, piece-wise, linear approach in order to obtain better performance. The results are that an initial timing variation of almost 3 μs has been reduced to a total variation of less than 100 ns.**

***Index Terms*—Excimer laser, magnetic pulse compression, magnetic switch, modulator, timing compensation, timing regulation.**

I. INTRODUCTION

THE CURRENT generation KrF excimer laser produced by CYMER is a 2-kHz version specifically designed for the application of photolithography. The laser is therefore integrated by our customers into a stepper or scanner that exposes the wafer with the integrated circuit image. One of the specific requirements from our customers is that the laser light should be generated 35 μs ± 100 ns after the laser receives a trigger signal. This requirement is needed because the stepper or scanner must synchronize the reading of data from a monitor that measures the laser light pulse energy.

In normal operation, the operating voltage of the solid state pulse power module (SSPPM) [1], [2] can range from 600 to 1150 V because the energy required by the laser chamber will vary as the electrodes wear, the gas becomes depleted/contaminated, and so on. This complicates the timing requirement because the magnetic switches saturate at earlier times at the higher operating voltages. A circuit has therefore been implemented to maintain a constant throughput delay in the SSPPM over the entire operating voltage range. The circuit operates by injecting a variable delay into the low-level trigger electronics between the SSPPM input and the switch triggering circuitry. Because temperature variations affect the magnetic switch volt-seconds, the circuit also adjusts delay for temperature variations.

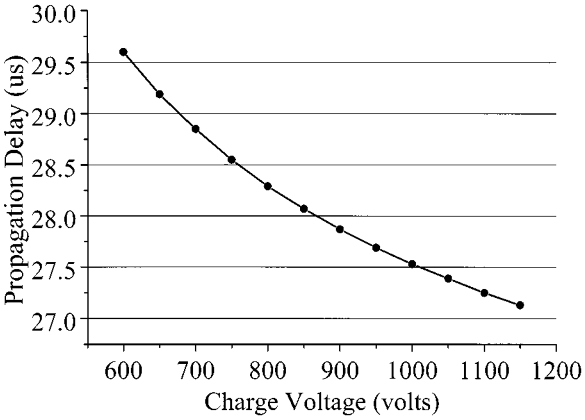

Fig. 1. SSPPM delay versus charge voltage.

After operating the SSPPM at 700 V, 2 kHz for 30 minutes, the system was within 99% of equilibrium temperature. As shown in Fig. 1, the trigger propagation through the system at the maximum voltage (1150 V) was 2.47 μs faster than at minimum voltage (600 V) at this particular operating temperature.

Compared with the earlier described requirement, a variation of 2.47 μs in propagation delay is unacceptable. The timing compensation circuit must therefore reduce the variation from this initial amount to the levels required by the laser, ±100 ns.

The latest SSPPM design uses two pulse compression stages. The compression time of the first stage is approximately 5 μs. The output stage compression time is approximately 600 ns. Overall, nearly 90% of the SSPPM pulse compression time occurs in the first stage reactor. Variations in the first stage reactor propagation time due to voltage and temperature are therefore the dominant changes in the total SSPPM propagation delay. The timing compensation circuit compensates primarily for these delay changes in the first stage reactor. Temperature feedback for thermally induced delay loss is measured exclusively near the first stage reactor housing.

II. TIMING COMPENSATION CIRCUIT

In order to compensate for the progressive loss of propagation time through the SSPPM at higher voltages, the initial charge voltage is sampled, and a corresponding delay is added into the low-level trigger circuitry. The propagation delay is an inversely proportional, nonlinear function of the initial charge voltage. An early timing compensation scheme corrected the loss of propagation time at higher voltages with a linear increase in trigger

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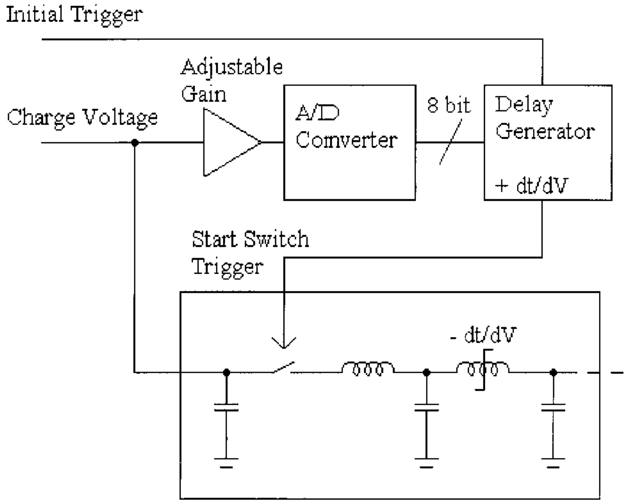

Fig. 2. Single linear compensation circuit.

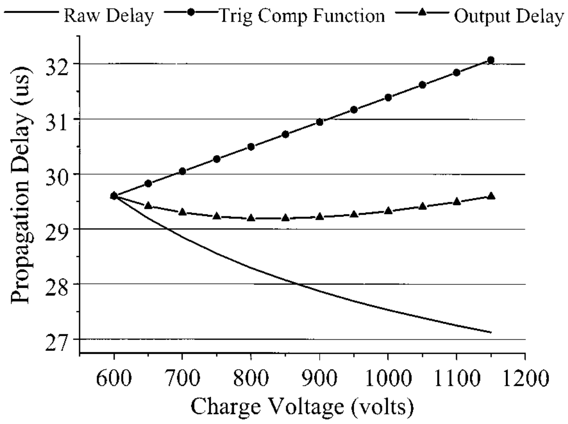

Fig. 3. Single linear compensation function.

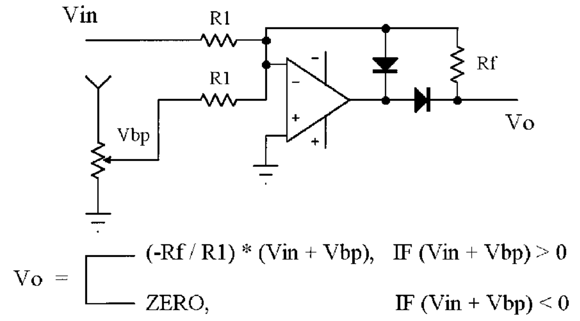

Fig. 4. Superdiode circuit diagram.

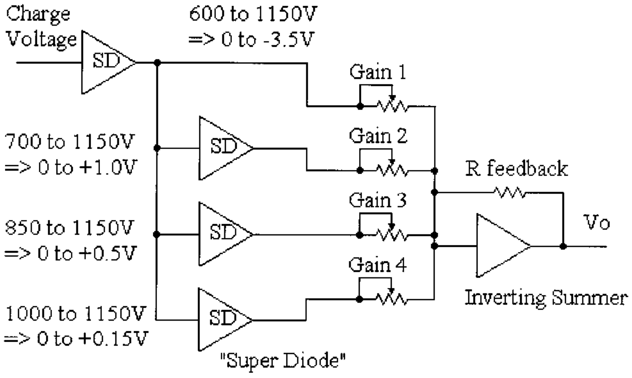

Fig. 5. Four-section piecewise linear circuit topology.

delay with respect to charge voltage. This "single linear" compensation circuit is outlined in Fig. 2.

Because the nonlinear delay characteristic of the SSPPM is compensated with a single linear function, the actual propagation function "bows" away from the linear compensation function, inducing an error in the regulation of the delay of the output pulse.

As shown in Fig. 3, the original single-linear compensation circuit is capable of reducing the initial delay spread of 2.47 μs to ~412 ns.

The ~412-ns error is the error associated with approximating the raw delay characteristic curve with a single linear function. Using multiple linear segments to construct a multiple piecewise linear compensation function can reduce delay regulation error. A four-section piecewise linear compensation circuit has been developed that regulates the output delay versus voltage to a window of approximately 42 ns. Because the most severe curvature in the raw delay function is in the lower voltages, the first linear section spans a smaller range of voltages than the upper three sections.

The basic building block of the four-section piecewise linear compensation circuit is the "superdiode" shown in Fig. 4. The op-amp yields zero output until the magnitude of the voltage at Vin exceeds the magnitude of the breakpoint voltage V_bp. Once V_{in} exceeds the preset threshold, the circuit "turns on." Each superdiode amplifier is an inverting amplifier.

In order to eliminate unit-to-unit variations in the charge voltage signal due to component tolerances, the primary superdiode block is adjusted to turn on at the minimum charge voltage, and the gain adjusted to yield -3.5 V at maximum charge voltage. This negative-slope function of the charge voltage is then split among three secondary superdiode stages, cascaded in parallel. Each subsequent stage turns on at the charge voltage determined by each respective breakpoint voltage. Each secondary stage inverts the slope of the primary stage.

All four voltage functions, the negative primary function, and three positive secondary functions are finally summed together at an inverting summer. The primary function sets up the primary slope of the compensation function. Each secondary stage cumulatively subtracts slope during each respective piecewise linear segment.

As shown in Fig. 5, the gain of each function is adjusted at the input to the inverting summer. Fig. 6 demonstrates the mathematical construction of the trigger compensation voltage function [slope $= -(m1 + m2 + m3 + m4)$]. Shown in the figure are the critical uncompensated raw data, the overall trigger compensation function, and each of the individual piecewise contributions to the overall compensation function.

Control over the gain of each contributing function allows the flexibility to adjust the timing compensation per each SSPPM unit. There is too much variation in the ΔB of the magnetic materials, and in the first stage CLC (capacitor-inductor-capacitor) transfer time to standardize the circuit gains. Both ΔB and the

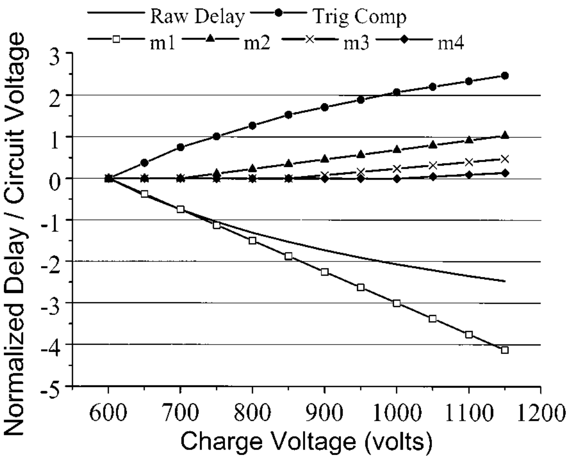

Fig. 6. Construction of four-section piecewise linear timing compensation function.

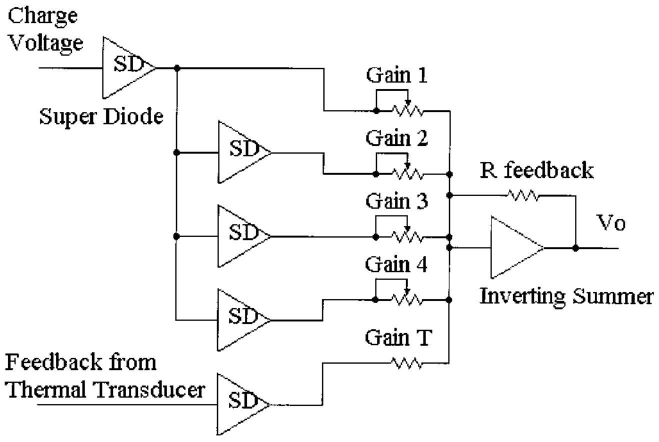

Fig. 7. Four-section piecewise linear timing compensation with direct thermal feedback.

CLC transfer time affect not only the magnitude of propagation delay, but also the curvature.

The four-section piecewise linear circuit compensates for propagation delay changes with respect to voltage. However, ΔB, and consequently the volt-second product, also changes with temperature. As the temperature of the magnetic switch increases, the propagation delay decreases. It is therefore necessary to shift the voltage compensation function, providing additional low-level trigger delay as a function of increasing temperature. This is accomplished by using thermal feedback from the magnetic switch, and another superdiode block appended to the summer junction as shown in Fig. 7.

Delay change due to temperature was regulated in the original single-linear compensation circuit with a low-pass RC network, charged up by the frequency of the start switch trigger. The time constant of the filter was selected to correlate with the thermal rise of the reactor. Although using a thermistor for direct thermal feedback in the most recent circuit design is better than the RC thermal approximation, it is still rather crude. Again, a nonlinear function is regulated by a linear function, inducing error. Error is also incurred from thermal lag between the center of the magnetic cores and the location of the thermistor, thermally linked to the reactor housing. However, because delay variation with respect to temperature is a relatively weak function, the direct thermal feedback approach is sufficiently effective. If left uncompensated, propagation delay varies almost 300 ns over the temperature range of the SSPPM. With direct thermal feedback, that 300 ns is reduced to 40 to 50 ns.

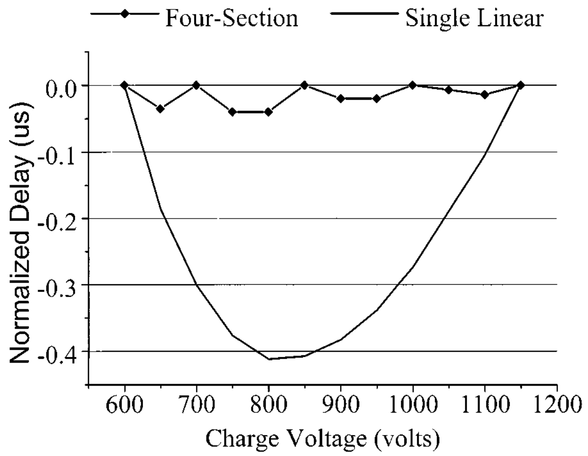

Fig. 8. Four-section piecewise linear vs. single linear delay regulation.

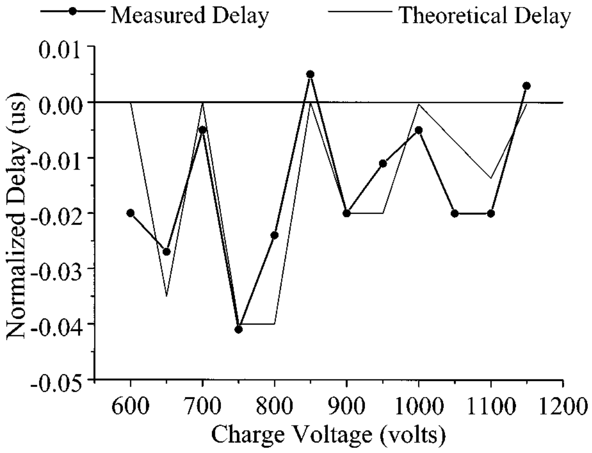

Fig. 9. Measured versus theoretical delay regulation.

III. CIRCUIT PERFORMANCE

We can compare the symmetry between the raw delay function and the multiple, piecewise linear trigger compensation function as shown in Fig. 6, with that of the original circuit data shown in Fig. 3. According to this mathematical model, a 10× improvement in delay regulation at one temperature is predicted. Fig. 8 demonstrates this expected improvement in propagation delay. Fig. 9 shows good correlation between theoretical and observed delay variation.

Indeed, measured results correspond well to theoretical predictions. The delay error of $\sim$412 ns associated with the original compensation circuit has been reduced to $\sim$42 ns. Over the thermal and voltage ranges of the SSPPM, the four-section linear compensation circuit regulates delay to a window of approximately 80 ns as shown in Fig. 10. For long-term, total system performance over typical voltage and temperature excursions, this corresponds to a 5× improvement in delay regulation.

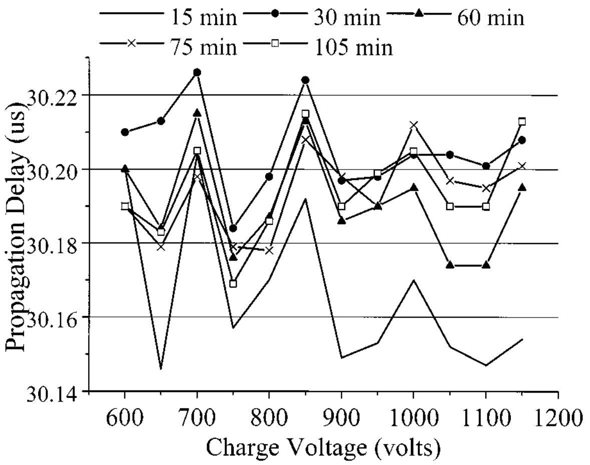

Fig. 10. Compensated propagation delay vs. temperature and voltage variations.

The delay compensation circuit is adjusted to its optimal setting after the SSPPM has been operated for 30 min at a moderate voltage (700 V), and full rep rate (2 kHz). The curvature of the delay function is slightly different in the thermal extremes; so voltage compensation is typically optimized near the midpoint. Because thermal compensation is such a weak function in comparison to delay compensation, the thermal delay gain is fixed, requiring no adjustment.

IV. SUMMARY

A four-section piecewise linear compensation circuit has been developed and implemented in the excimer laser SSPPM that regulates the throughput propagation delay time from the SSPPM trigger-to-laser light output. The uncompensated propagation delay varies up to 3 μs with 90% of that variation due to changes in voltage, and 10% due to changes in temperature. The four-section compensation circuit reduces delay variation to ± 20 ns over all charge voltages, at the steady-state temperature. Delay regulation is ± 40 ns over the total temperature and voltage range. Overall, this is a 5× improvement in delay regulation compared with the original single-linear compensation circuit.

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David Johns (S’97–M’98) received the B.S. degree in electrical engineering from the University of Missouri at Columbia.

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