HIGH POWER SWITCHING USING POWER FET ARRAYS

G.T. Santamaria and R.M. Ness
Maxwell Laboratories, Inc.
8888 Balboa Ave.
San Diego, CA 92123

Abstract

This paper describes the design and use of a switch array of 2400 power FETs to produce 6 kV, 700 A, 3 μs pulses at repetition rates up to 60 kHz. The choice of power FETs over other switch candidates and the array sizing considerations are examined. The array is composed of 40 series-connected, multi-layer, printed circuit card assemblies, each containing 60 parallel devices. Fiber optics are employed to deliver the gate drive signals to each of the cards as well as to return a switching verification signal to the control electronics. Finally, operational performance data are presented and discussed along with practical limitations for operation outside the design range.

Introduction and Modulator Switch Selection

The purpose of this project was to design and develop a switch to modulate the output of a 6 kV, 80 A dc power supply. The initial design requirements for this switch are listed below in Table 1.

Table 1
Modulator Switch Requirements

Voltage:	6 kV
Peak Current:	700 A
Average Current:	80 A
RMS Current:	150 A
On-Time:	31.3 - 180 μsec
Off-Time:	1.7 - 90 μsec
Frequency:	DC - 60 kHz
Current Rise Time:	500 nsec
Current Decay Time:	3 μsec (e-fold)
dI/dt:	1400 A/μsec minimum

Many different switch technologies were reviewed during the design selection process. Potential candidates for this switch included: thyratrons, hard tubes, thyristors, bipolar power transistors, and power FETs. The hydrogen thyratron, if force-commutated, would have recovery times which are marginal. Furthermore, little has been done to characterize large thyratron operation at high pulse repetition frequencies. The vacuum tube, either a triode or tetrode, has many desirable properties; however, its characteristically high voltage drop is a serious drawback which would result in high power losses for the system. When operated in high-duty cycle circuits at low load current, vacuum tubes tend to have excessive grid dissipation. Thyristors exhibit some significant potential; however, high dI/dt (>500 A/μsec) operation is accomplished only with asymmetric type devices. Smaller sized asymmetric devices exhibit good turnoff times (4 - 7 μsec), while larger devices with higher current and voltage ratings have insufficient recovery times. Both thyristors and thyratrons require additional commutating circuitry which can reduce reliability, complicate control and greatly increase troubleshooting difficulties. The bipolar power transistor is unsuitable because of the broad unit-to-unit variation in turnoff delay (storage time) and turnoff times. Although large numbers of devices would be required to meet the switch voltage and current requirements, power FETs have several advantages over other solid state devices. Gate drive requirements are modest and series and parallel operation are relatively simple, the latter made easier by the positive temperature coefficient of the on state resistance, $R_{DS\ ON}$. Therefore, the power FET, with its high speed and low on-state voltage, has been chosen.

Design Considerations

Component Selection

A number of different FET devices were considered with respect to cost per rated volt-ampere product. At rated drain-to-source breakdown voltages (BV_{DSS}) in excess of 500 V, devices tend to have high on state resistances (R_{DSON}) and low rated current per unit chip area. Thus, device selection was limited to those with BV_{DSS} ratings of 500 V. Packaging considerations also favored those devices in a TO-220 case, as opposed to a TO-3 case, due to the easier assembly procedures required. The 500 V, 8 A, TO-220 packaged IRF840 device was therefore chosen because of its performance specifications meeting these criteria.

Array Sizing

As shown in Figure 1, the devices are arranged in an N_S x N_P series-parallel array of devices, each device having:

$$V_{DS} = \frac{V_{ADS}}{N_S} \qquad I_D = \frac{I_{AD}}{N_P}$$

when currents and voltages are shared equally amongst all of the devices. Current sharing is an inherent trait of power FETs when connected in parallel provided that the devices within a parallel group operate at the same case temperature [1]. Dynamic current sharing occurs because those parameters affecting dynamic performance typically vary from device to device by no more than 20%. Static or dc voltage sharing is enforced by connecting a resistor in parallel with each FET. The peak voltage across each device is limited by a series-connected pair of zener diodes, also connected in parallel with the FET and located close to the device to minimize the effects of stray inductance. These zener diodes are selected so that the maximum clamping voltage never exceeds 75% of rated BV_{DSS} for the power FET, resulting in a 380 V clamping level (for the 2 series connected diodes). Such devices have a rated standoff voltage of 2 x 100 V. The dc level for each FET is set to be 75% of the zener diode standoff, or 150 V. Therefore, the array requires that:

$$N_S = \frac{6000}{150} = 40$$

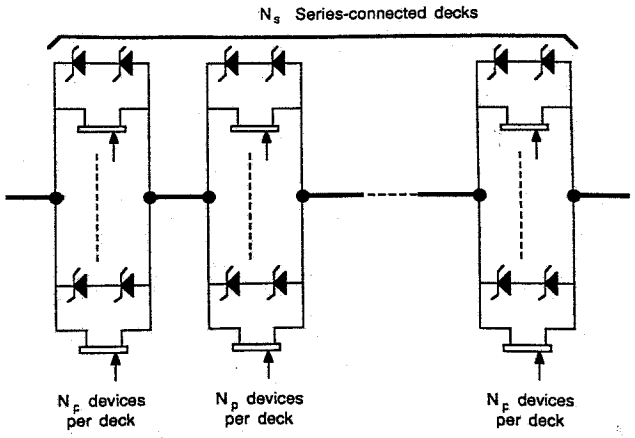

Figure 1: Simplified schematic showing the interconnection of FET devices to form a high power array.

The number of parallel-connected devices on each series board, N_P, is driven by three considerations:

- Reliability - a higher current per device results in a higher junction temperature which, in turn, results in a higher failure rate per device.
- Fault current - the maximum pulsed drain current ratings of the FETs must not be exceeded under any circumstances.
- Efficiency - fewer devices mean higher switch losses which, in turn, imply higher system operating costs.

Efficiency is a consideration for life cycle operating cost. Tradeoffs comparing the increased additional cost of more devices against the increase in life cycle costs due to higher system power losses favor a larger number of parallel devices in the initial switch array sizing. In the design of the overall modulator, the fault current is limited to 1500 A and thus, 60 parallel devices provides a sufficient safety margin to ensure that the device maximum current rating of 28 A is not exceeded.

Gate Drive

Transformer isolation of gate drive signals is commonly employed in smaller systems using power FETs. Typically, the primary side of the transformer is driven by some type of bipolar or FET circuit and one or more secondaries is connected through a network comprised of diodes and possibly small FETs to the gate of the driven output FET. Driving 60 parallel devices in this manner, with a 100 ns risetime to a voltage of +8 V, requires that the transformer and driver source have an equivalent output resistance of 0.3 ohms and an inductance approaching 3 nH. Further complications arise from the high duty cycle (up to 90%) requirement of the this switch application. Thus, our FET array design employs a fiber-optic-coupled circuit. Driving the FET gates in this manner yields three key advantages for the system design:

- Dc coupling avoids complications due to transformer saturation, important in high duty-cycle (>50%) operation and allowing the gate drive circuitry to operate with pulse repetition rates from dc up into the Mhz range.
- The FET gates remain shorted to the source after device turnoff. This makes the device more immune to dv/dt effects in the off state.
- The ground level control electronics can be fully isolated in a simple manner from the power FET boards, eliminating conducted EMI coupling.

Instability Suppression

Parasitic instabilities which can occur in parallel operation are due to the stray inductances associated with the FET leads and package. Such instabilities generally manifest themselves as ringing in the V_{DS} and V_{GS} waveforms during switching. Analysis has shown that some small series resistance (typically 5 ohms) in series with the gate lead and a careful layout of the gate circuit will eliminate such oscillations [2].

Power FET Array Assembly

The array was built from a set of 40 series-connected printed circuit boards, each containing 60 parallel power FETs. In order to meet the current risetime requirements of the switch assembly, these printed circuit boards were built using a multi-layer construction to minimize switch inductance. The first two conducting planes were dedicated to the power FET drain and source connections and are separated by a distance of 0.016". The two remaining planes are used for routing gate drive signals and other board diagnostic functions. Each of the 40 board assemblies measures approximately 20" x 20" and includes 3 water-cooled, cold plate heat sinks attached to cut out areas of the boards. Twenty output power FETs are then mounted on each heat sink, which is electrically tied to the FET drain plane. This method of heatsink mounting lends a great deal of stiffness to a large surface area printed circuit board while maintaining a thin overall profile.

As mentioned previously, the gate drive signals for the output power FETs are transmitted to each card through fiber optics. The fiber optic signal is generated in low-level logic circuitry and transmitted via low cost plastic fiber optic cable to a fiber optic receiver located on each FET board. The TTL output signal from the receiver is then amplified in a three stage primary driver circuit comprised of several DMOS FETs. The output of the primary driver stage is then further amplified in three parallel intermediate driver stages, each of which provides the gate drive signals for twenty output power FETs. These intermediate drivers, as well as the final stage of the primary driver, use DMOS FETs which are connected in complementary fashion resembling CMOS integrated circuits. An onboard +8 V power supply, fed from a multiple secondary winding isolation transformer, provides the necessary power to each board for these gate drive circuits and other board diagnostics.

Each output power FET cell contains a variety of key components, most of which were discussed briefly in the previous section. A more detailed description of the circuit, as shown in Figure 2, is given here. The input to the FET is through a 4.7 ohm resistor, R1, selected to minimize the chance of parasitic instabilities. A 1/2 amp fuse is also connected in series to guard against the possibility of a FET failing with a gate-source short. In the event that this does happen, the intermediate driver can supply sufficient current to blow the fuse and isolate the failed FET cell from the remainder of the circuit. A zener diode is also connected in parallel with the gate-source of the FET to protect against voltage spikes being applied to the gate.

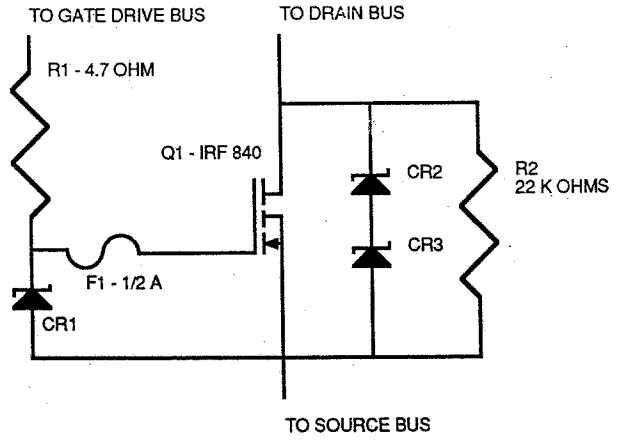

Figure 2: Schematic diagram of output power FET cell showing key components.

To aid in static voltage sharing among the 40 FET boards, a voltage grading resistor, R2, is connected in parallel with the output FET drain-source. A pair of transzorbs (zener diodes) are also connected in parallel to ensure that damaging voltage spikes are not applied to the FET.

One of the primary diagnostics built onto each board is a circuit which determines whether or not the board has switched on or off by monitoring the voltage across the power FET drain-source buses and comparing it with a predetermined threshold. This switch detection circuit then relays this board status signal back down to the ground level control electronics via the same type of fiber optic link as used for bringing the gate drive signal up to the board.

Operational Data and Results

This original FET board design was prototyped by building three units and examining them in a series of tests. The prototype

test stand, shown in schematic form in Figure 3, was designed to prove basic card operation up to the design limits of switching 150 V per card and 700 A peak current. Since electrical power from the power supply/filter capacitor was limited, testing was done in "burst mode" style. The FET gate drive circuitry was successfully operated from dc up to 1 Mhz repetition rates, while the entire FET board was run from 5 - 100 kHz. By comparing the current risetime while operating with 1 card and with 3 cards, it was determined that the risetime (500 ns) was not degraded by adding cards (and therefore card inductance was negligible compared to that in the test stand itself). Voltage grading, both at dc levels and during the dynamic switching times, was examined and found to be within acceptable limits. Current and voltage waveforms for one card can be seen in Figures 4 and 5. Results from these prototype efforts proved the basic concept of the design.

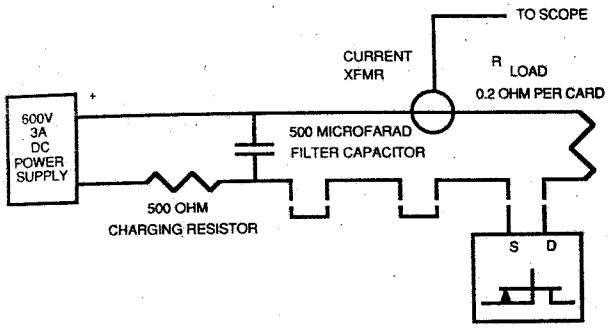

Figure 3: Schematic diagram of FET board test stand.

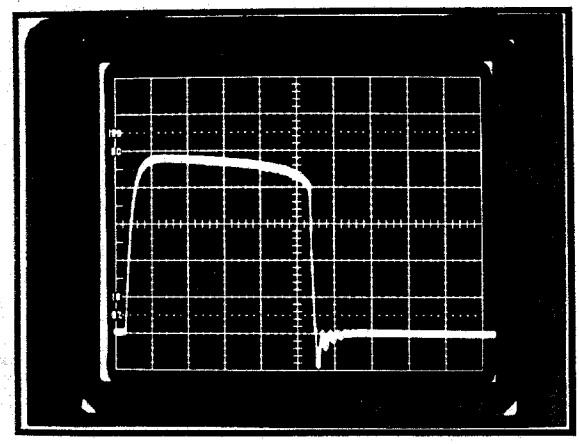

Figure 4: FET board current waveform (1 µsec/div and 94 A/div).

This same test stand was then modified by replacing the power supply with a higher power model (60 kW), increasing the load power capacity, and adding cooling water facilities for removing heat from the card heat sinks. These modifications were performed in order to test the boards at the full design average power levels. Some failures of the transzorb pairs occurred during the initial phase of this test period. Because the test stand load was primarily resistive, the switched current at FET turn-off was still very close to the peak value of 700 A. At turn-off, the energy due to this current flowing in the test stand inductance had to be dissipated in the card, thereby overstressing the design ratings of the transzorbs. In actual operation in the overall system, the current at turn-off is much less due to the capacitive nature of the system load. Thus, the test stand operation was a "worst case" scenario for examining switching operation. This situation was later rectified by inserting a capacitance in series with one half of the load resistance. As a result, the load current at turn-off was reduced to below 350 A, while the peak and RMS currents were maintained. Each of the 40

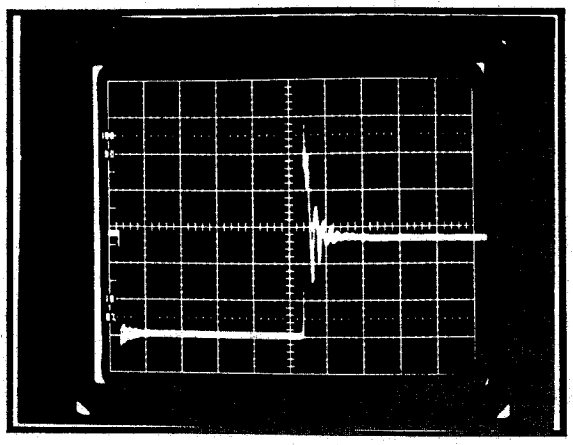

Figure 5: FET board voltage waveform (1 µsec/div and 50 V/div).

production FET boards was then run at 30 kHz rep-rate and near maximum design power levels, for 8 hours. No FET failures occurred during this testing. A current waveform from the testing can be seen in Figure 6.

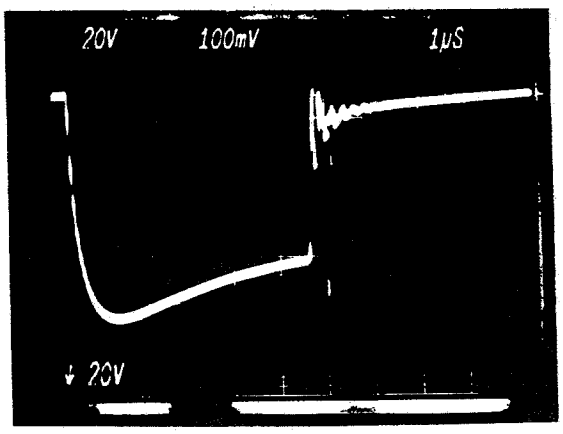

Figure 6: FET board current waveform in modified test stand (1 µsec/div and 100 A/div).

Summary and Conclusion

An array of 2400 power FETs has been successfully designed and built to modulate a 500 kW average power dc power supply at repetition rates up to 60 kHz. This array is composed of 40 series connected, multi-layer printed circuit boards, each of which contains 60 parallel power FETs.

The operation of these FET boards has met or exceeded all of the critical design goals, including switched voltage, peak current, RMS current, average current, and rep-rate. As was mentioned in the previous section, the gate drive circuitry has been operated up to 1 Mhz while the card itself has run at frequencies of up to 100 kHz. Since other device design parameters are conservatively rated, such as the FET drain to source voltage and peak current ratings, these operational variables may be extended past the design goals as well. As long as the maximum device limitations are not exceeded, as in the case of the transzorbs, and if slightly reduced board reliability is acceptable, this array should be capable of operating at much higher power levels.

References

[1] Severns, Rudy, "Parallel Operation of Power MOSFETs", Siliconix Application Note TA-45.

[2] Ibid.