0.5 MW 60 KHZ SOLID STATE POWER MODULATOR

R.M. Ness, E.Y. Chu, and G.T. Santamaria*
Maxwell Laboratories, Inc.
8888 Balboa Ave.
San Diego, CA 92123

Abstract

This paper describes the design, construction, and test results of a 0.5 MW average power solid state modulator which produces square pulses at variable voltages up to 5.5 kV and repetition rates up to 60 kHz. This modulator generates current pulses with peak amplitudes of 700 A and risetimes of less than 500 ns (10-90%) into a nonlinear load which is also subject to frequent open circuit or short circuit faults. The system consists of three subsystems: a high voltage dc power supply subsystem, a modulator subsystem, and a controls subsystem. The dc power supply subsystem is capable of producing 6 kV, 80 A dc and consists of a SCR phase controlled, 12-pulse transformer/rectifier set, filter capacitor, and crowbar. The modulator subsystem includes a saturable reactor for fault current limitation, a series switch, and a shunt switch. The series switch is constructed of a series/parallel array of 2400 Power MOSFETs whereas the shunt switch uses a smaller array of 400 of the same devices. Electronics in the controls subsystem operate and monitor the dc power supply and the two modulator switches. In the case of a fault, the system is shut down in a safe manner by opening the switches, phasing back the dc power supply, and if necessary, firing the crowbar ignitrons. Control functions are provided through a local control panel and an isolated computer interface. The results from the testing of the modulator are presented and practical limitations to operation outside the design parameter space are also discussed.

Background

System Description

The purpose of this project was to design a 0.5 MW average power modulator with the major parameters shown below in Table 1. This pulsed power system was expected to operate for periods of up to 400 hours continuous running time. Reliability and long lifetime were therefore important goals in the design considerations as well as high efficiency and maintainability.

Table 1
Modulator Requirements

Voltage:	-500 V to -5.5 kV
Peak Current:	700 A
RMS Current:	150 A
Average Current:	80 A
Pulse On-Time:	16 to 256 μsec
Pulse Off-Time:	1.6 to 256 μsec
Pulse Frequency:	DC or 5.5 to 60 kHz
Current Rise Time:	500 nsec
Current Decay Time:	3 μsec (e-fold)

The design load for the power modulator was expected to be nonlinear and also subject to frequent load short circuit faults (up to 100 per minute). During such a fault, the modulator was designed to operate in one of two modes. In the manual mode, the system would merely shut down upon detection of an overcurrent condition. In the automatic recovery mode, the system would shut down for a preset time interval and then return to normal operation with the operating parameters which were in effect prior to shutdown.

The rise time requirements for this pulsed power system necessitate a minimum di/dt of 1400 A/μsec at the 6 kV output level. This also implies that if a load short circuit occurs, the fault currents may rise to values on the order of 9 kA before the diverter is able to fire. Sizing the solid state modulator switch arrays to handle these possible fault currents would have resulted in prohibitive costs. Therefore, a method was devised for limiting the peak fault currents by using a biased saturable reactor which would present a low series inductance to the system during normal operation and a high inductance during fault conditions. This technique will be discussed more in the section dealing with the modulator design.

Shown in Figure 1 are the two major assemblies for the power modulator during factory testing at Maxwell. In the background is the enclosure which houses the input ac switchgear, SCR phase controllers, and transformer/rectifier set. The other assembly is split into two, with the Modulator enclosure mounted on top of the Diverter/Filter. The front section of the Diverter/Filter enclosure contains the filter capacitor bank, ignitron diverters, and magnetic limiter while the rear contains electronic chassis and auxiliary systems. The front panel of the diverter trigger generator can be seen in the window in the lower left corner. The rear half of the Modulator enclosure is almost completely taken up with the series switch array. The front half of the cabinet contains two control panels, for operating the dc power supply and modulator subsystems, and the shunt switch array.

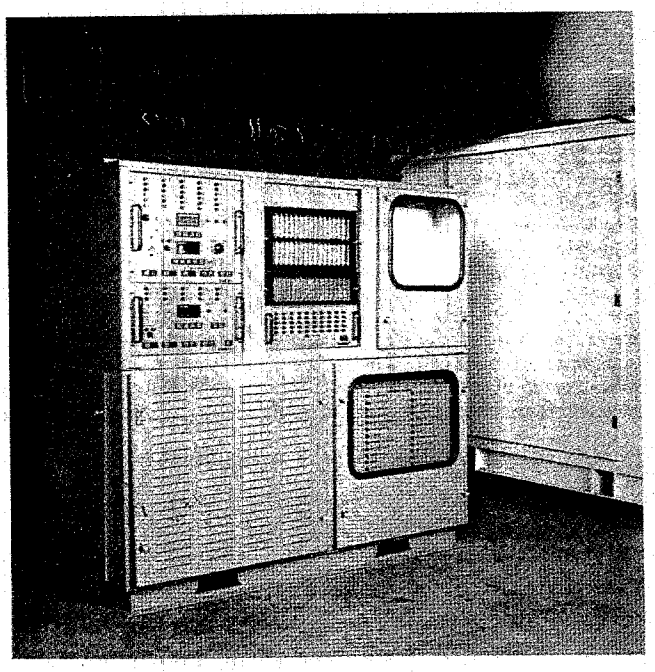

Figure 1: Modulator mounted on top of the Diverter/Filter with the T/R set enclosure in the background.

Design Trade-offs

Modulators can generally be divided into one of two broad classes: the "line" type or the "hard tube" type. The former is made up of a Pulse Forming Network (PFN), charged from a charging source and discharged by a closing switch into the load. The output pulse characteristics depend strongly on the load and some or all of the PFN component must be modified to change the pulse shape. The "hard tube" modulator is so named because a vacuum tube is typically used to switch a "stiff" voltage source into the load. Because of the wide range of desired pulse lengths and the expected characteristics of the nonlinear load, the latter type modulator approach was selected.

* Presently with G.A. Technologies, San Diego, CA.

Of the many different potential candidates for the modulating switch, power MOSFETs were chosen because of their high speed, low on-state resistance (and therefore higher efficiency), and low gate drive requirements. Although a large number of devices were required for this application, series and parallel operation of MOSFETs are relatively simple, the latter made easier by the positive temperature coefficient of the device on-state resistance, $R_{DS\ ON}$.

An additional trade-off which was addressed concerned the method for providing the gate drive signals to the MOSFETs. After considering several different transformer coupled methods of distributing these signals, it was decided to use fiber optics instead since they would allow smaller size, wider bandwidth, and better isolation. This technique also allows a one-to-one correspondence between the low level logic which drives the fiber optics and the MOSFET status.

Power Modulator Design

DC Power Supply Subsystem

The 6 kV, 80 A, regulated dc power supply subsystem is made up of the input switchgear, SCR phase controllers, Transformer/Rectifier (T/R) set, capacitor filter, and ignitron diverters.

The input ac switchgear consists of a 480 V, 800 A frame circuit breaker and fast acting, current-limiting semiconductor fuses. Both are designed only as a redundant measure in the case of a failure of either an SCR or the control electronics since in the case of a fault, the SCRs will be immediately phased back. The circuit breaker also includes a shunt trip coil, for fail-safe opening in the case of loss of power, and a motor operator for remote closing and opening of the breaker. Fuse characteristics were chosen such that the circuit breaker will open prior to fuse melting except in the case of a fault on the primary side of the T/R set.

Twelve-pulse phase control was chosen so that the output filtering requirements and input current requirements were reduced. In this configuration, two separate transformers are used. The first is built with a delta-wye winding such that the secondary line to line voltage leads the primary by 30 degrees and the second transformer has a delta-delta winding. The three-phase rectifier bridges are connected in series to form the output and the 30 degree phase shift between the two provides the 12 pulse operation. A 12 percent transformer impedance was selected, primarily because of manufacturing economics, and additional series inductances were then added to minimize possible fault currents.

A 570 μF filter capacitor bank is provided to store sufficient energy to reduce the voltage sag which occurs during power supply turn-on to acceptable levels. This capacitance also assists in the filtering of output voltage ripple, which can become moderately large when operating such a phase controlled system at low output voltages.

Two size D ignitrons are used to safely discharge the stored energy in the filter capacitor bank and the T/R set. In the case of a load fault and a failure of the modulator switch arrays to open, a fiber optic signal is sent from one of two isolated current shunts and comparator circuits to each of the two independent trigger generators. This signal is then amplified through a series of FET stages which drive a thyratron, discharging a capacitor through the primary of a step-down trigger transformer. The output of the trigger transformer then drives the ignitor of the ignitron.

Modulator Subsystem

Major components in the modulator subsystem include a series switch, a shunt switch, and a magnetic limiter. A simplified schematic diagram of the modulator subsystem is shown in Figure 2.

The series switch is made up of an array of 2400 power MOSFETs. IRF-840 devices, rated at 500 V and 32 A peak current, were selected for this application. Sixty such devices are connected

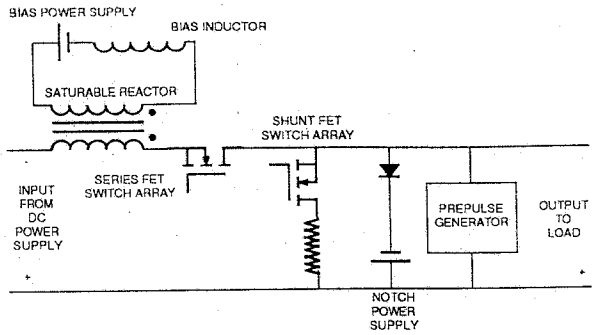

Figure 2: Simplified schematic diagram of the Modulator subsystem.

in parallel on each of the 40 series-connected printed circuit board assemblies. Thus, for high reliability and long lifetime, each power MOSFET is conservatively designed to operate at conditions of 150 V and 11.67 A peak current. The TO-220 cases are physically mounted to three water cooled heat sinks mounted over cutouts in the 19.5 in. x 17 in. circuit board. Multi-layer construction was employed in fabricating these printed circuit boards in order to minimize the inductance associated with the switch assembly. As shown in Figure 3, each board is slid into a horizontal card cage assembly with a motherboard providing connections from card to card. A fiber optic trigger from ground level electronics is delivered to the top edge of each board and then amplified and distributed on the board through a set of MOSFET intermediate drivers. Power MOSFET status (open or closed) is also monitored by a comparator circuit and transmitted back to the control electronics through a second fiber optic link. Input and output water connections for the heat sinks can be seen at the bottom of the figure. These switch assemblies are described in greater detail in another publication [1].

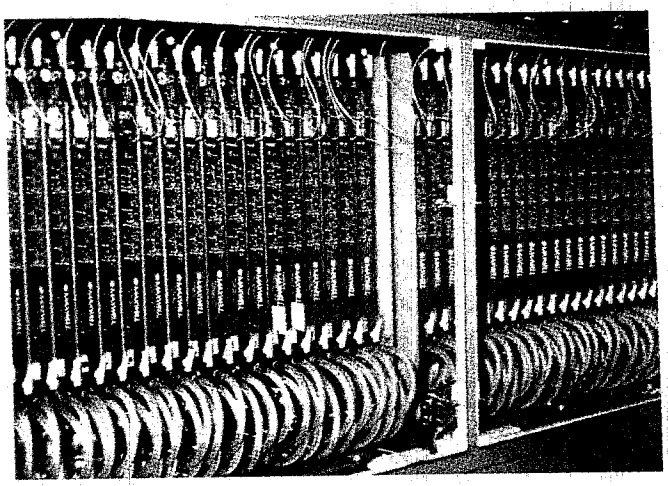

Figure 3: View of the Series FET switch card cage assembly with cards in place.

The shunt switch, made up of a similar array of power MOSFETs, is used as a "tail-biter" to improve the voltage falltime of the output pulse. However, because the current requirements for this switch are lower than that of the series switch (100 A peak versus 700 A peak), the number of parallel devices is reduced to 10 and four separate series-connected sections are assembled on each card assembly. Ten cards then provide the full 6 kV switch array capability. A power resistor is also placed in series with the shunt switch to absorb the energy stored in the cables which deliver power to the load.

The magnetic limiter is made up of a saturable reactor, a bias inductor, and a bias power supply, rated at 10 V and 165 A. This reactor is normally operated in the negative saturation portion of the B-H curve, allowing a minimal inductance of approximately 250 nH to be placed in series with the load. During a load fault condition,

the current rises sufficiently to bring the reactor out of saturation, at which point the effective inductance increases, limiting the fault di/dt to a much lower rate. The diverter is then fired during the time the reactor is out of saturation and voltage is removed from the circuit, allowing the fault current to decay. The saturable reactor toroidal core is wound with nickel-iron tape and designed for a 21 x 10^{-3} volt-second product. The bias winding has ten times the number of turns as the main winding to minimize the bias current requirements. Thus, with a bias current of 100 A, the current limit threshold where the reactor will come out of saturation is 1000 A and the current rises to approximately 1200 A at the end of the 3.8 μsec holdoff period. This threshold can be adjusted by varying the current from the bias power supply. The bias winding is divided into two sections and interconnected with the two 9 mH inductors which make up the bias inductor. This allows realistic insulation requirements on the bias circuit since transients of up to 60 kV (ten times the full modulator output of 6 kV) can be impressed when the modulator switches off.

An additional Notch Power Supply, rated at 150V and 18 A, is supplied to provide a small bias to the load during the period when the series switch is turned off and the main dc power supply is removed from the load. Finally, a Prepulse Generator is also included in the modulator to generate a 200 μsec pulse of up to 700 V amplitude prior to turning the series switch array on at the beginning of each pulse burst or continuous run.

Controls Subsystem

The controls subsystem is made up of two local control panels, a computer interface, and several electronic chassis. The two local control panels allow complete control and monitoring of the dc power supply and modulator subsystems. Potentiometers allow setpoint control for output voltage, pulse on and off time, and several other parameters. Other switches, meters, and indicators are provided to select and monitor system parameters and display interlock status.

Selected parameters from the control panels are then used to provide input to the electronics chassis which control either the dc power supply or the modulator. A feedback loop in the dc power supply controls monitors the T/R set output voltage and adjusts the SCR firing angles such that the output matches the desired setpoint. In a similar manner, pulse shape information (on and off time) is used in the modulator electronics to derive a master gate signal to drive the series switch array. This signal is then complemented to provide a gate signal for the shunt switch array. These signals are then transferred to a separate chassis which is used to split the signal into the individual fiber optic signals required by each series FET switch board and each shunt FET switch group. FET status signals are also received by fiber optic receivers and compared with a time-delayed gate signal to verify proper switch operation.

A computer interface allows complete remote operation of the pulsed power supply system from the customers facility computer control system. These two electronics chassis also isolate the pulsed power supply from the computer system in order to eliminate the possibility of introducing EMI into the system at this point. Discrete monitor and control signals are isolated through 24 V dry contact reed relays. Analog setpoint and monitor signals are isolated with Voltage/Frequency (V/F) and Frequency/Voltage (F/V) conversion techniques and fiber optics. Voltages (or currents) are first converted into a pulse train, whose frequency is proportional to the input level. A 0 to 10 V voltage level, or 4 to 20 mA current level, corresponds to a 5 to 25 kHz pulse train. This pulse train is then transmitted over a digital fiber optic link and converted back into a voltage or current level at the receiving end. V/F and F/V conversion is also used internal to the system to transmit analog signals between the T/R set enclosure and the Diverter/Filter and Modulator enclosures since the physical distance between the two locations is approximately 500 feet.

As with the other subsystems in the pulsed power supply, the controls are required to perform reliably in a high EMI environment. Single point grounding was adopted and twisted shielded pair cables were used for all "hard" wiring. Relays, opto-isolators, and fiber optic links were used for isolation of signals and sensitive electronics were built in shielded portions of the chassis with EMI filtering on the input/output connections.

Because much of the controls circuitry was of a repetitive nature, modular printed circuit boards were designed for all of the major electronics functions, including interlock monitoring, setpoint generation, metering, and on/off/reset control with local/remote selection. This made construction easier since the chassis level wiring was reduced and serviceability was improved because of the easy replacement and limited required troubleshooting in order to trace problems. Sensitive electronics could also be partitioned and isolated from other circuitry.

Safety and Fault Protection

Numerous interlocks were designed into the pulsed power supply for both system equipment and personnel safety, including redundant enclosure access and HV lockout switches. Interlocks also verify proper readiness of the diverter and the magnetic limiter by monitoring the diverter trigger generator and the magnetic limiter bias current. Other critical system conditions which are monitored by interlocks are blown fuses, ac and dc overcurrents, dc overvoltage, loss of regulation, loss of cooling functions, ac loss of phase, smoke alarms, and control electronics failures. All interlocks must be satisfied prior to closing the primary circuit breaker and in the case of an interlock opening or a loss of power, fail-safe control logic operation ensures that the breaker is tripped and the output dump and grounding relays in all enclosures are closed.

Other control logic monitors the status of both the series and shunt FET card assemblies. As mentioned in the previous section on controls, a status signal is returned via fiber optics from each FET card which relates the status (switched open or closed) of each series FET section back to the control electronics. This signal is then compared with the gate drive signal and any anomalies are flagged and displayed. In the case of a switching fault where the MOSFETs do not close, the system is immediately shut down and the fault annunciated. In this case, further operation would subject that card to the total voltage applied across the switch (when the remaining FET cards closed) resulting in further substantial damage to the card. In the case of a card failing to open, the system also annunciates the fault but does not shut down until a number of sections fail in this manner. This type of fault will result in a slightly higher voltage impressed upon each series section during the open state since there is one less to support the full voltage. Since the MOSFETs are conservatively rated, a modest increase in operating voltage is acceptable. When a sufficient number of sections fail and the voltage across the remaining MOSFETs becomes unacceptable, the system is shut down.

The SCR firing cards, loss of phase relay, and other support components which require 480 V power are all fused with pin type indicating fuses in order to make troubleshooting easier and also to provide safer isolation from the 800 A, 480 V primary service.

Redundant systems are also designed into the modulator to ensure survivability. It has been mentioned previously that the design load for this application is quite susceptible to short circuit faults and that the design has included a magnetic limiter to minimize the increase in fault current for a period of approximately 4 μs while the FET switch arrays have sufficient time to open. During a load fault condition, a high bandwidth current shunt monitors the output current and detects when the overcurrent threshold has been exceeded. A signal is then sent to the control electronics to open both the series and shunt switch arrays. If the overcurrent condition persists after 1.6 μs have elapsed, a signal is sent to each of the two diverter trigger generators to fire the ignitron diverters. A second backup current shunt also monitors the current and sends another trigger signal to both diverter trigger generators if the condition still persists after another 1.6 μs. Thus, there are two complete redundant diverter units from sensor to ignitron diverter.

The redundancy continues through the dc power supply subsystem. The same signal from the current shunt is used to inhibit SCR firing. Slower responding interlock signals from current transformers and a Hall probe monitor for both ac and dc

overcurrent conditions in the dc power supply and in the case of a fault, the breaker is "manually" opened by the shunt trip coil. If these actions fail, the fault may still be eliminated by the circuit breaker tripping or the primary fuses blowing.

Operational Data and Results

A substantial amount of testing was performed on the power modulator, both "in-process" during the fabrication and after final assembly had been completed. Many of the controls circuits and chassis were tested prior to integration into the overall system. Series and shunt FET printed circuit cards underwent "burn in" testing by operating each card in a specially constructed test stand at approximately full power ratings for a period of 8 hours. The dc power supply subsystem was also tested as an independent unit and operated into a resistive dummy load at full power (6 kV and 80 A) for an 8 hour period.

Checkout at the system level was then performed to verify proper operation and integration of the various subsystem units. Figure 4 shows the prepulse generator output pulse during the modulator turn on sequence. Many of the fault protection systems were also tested during this phase, such as the magnetic limiter and the diverter.

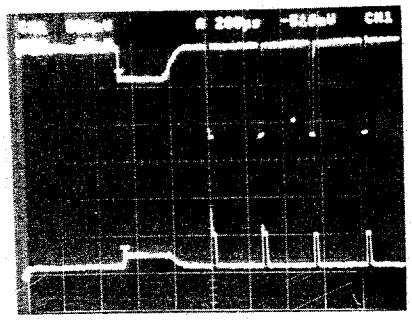

Figure 4: Prepulse generator output voltage waveform (top trace: 200 µsec/div and 500 V/div) and output current waveform (bottom trace: 20 A/div).

After integration of the entire system was completed, characterization of the power modulator began. This was done by varying different operating parameters such as the output voltage, load impedance, pulse frequency, etc. Figures 5-7 show one of the sets of data collected during operation at 5500 V, 346 A peak (144 A rms), and 9 kHz. Figure 6 is an expanded view of the risetime of the output voltage waveform of Figure 5. Figure 8 displays the output voltage and current measurements made during operation at 60 kHz.

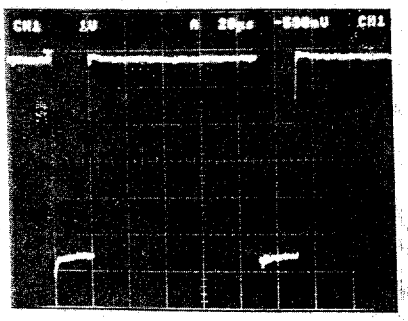

Figure 5: Power Modulator output voltage waveform (20 µsec/div and 1000 V/div).

Because operation into a purely resistive load would not allow simultaneous testing of peak, rms, and average current, most of the testing was done with regard to the latter two. In order to investigate peak current capability, some capacitance was added in parallel with the load. Figure 9 shows the resulting waveforms with the current reaching a peak value of over 500 A.

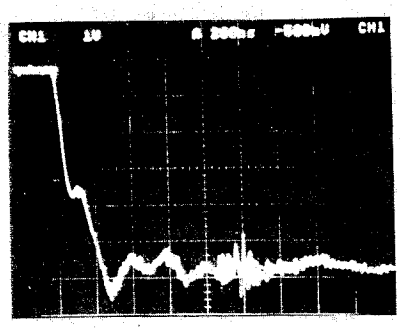

Figure 6: Power Modulator output voltage waveform showing risetime detail (200 nsec/div and 1000 V/div).

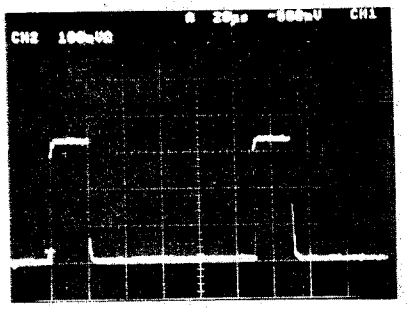

Figure 7: Power Modulator output current waveform (20 µsec/div and 100 A/div).

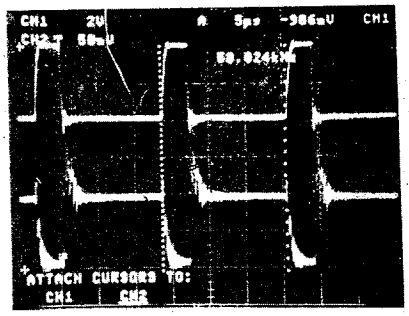

Figure 8: 60 kHz operation of Power Modulator showing output voltage waveform (top trace: 5 µsec/div and 2000 V/div) and output current waveform (bottom trace: 50 A/div).

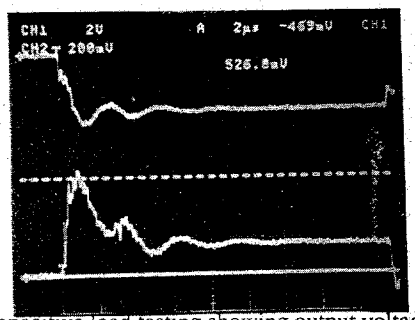

Figure 9: Capacitive load testing showing output voltage waveform (top trace: 2 µsec/div and 2000 V/div) and output current waveform (bottom trace: 200 A/div).

Upon completion of the power modulator characterization and preliminary testing, the unit was run for 40 continuous hours as an acceptance test. No major failures occurred and the system was disassembled, packed, shipped, and installed at the customers facility. A similar checkout and 12 hour full power test were then completed for final acceptance.

Summary and Conclusion

A high average power modulator has been successfully designed and built to modulate a 500 kW average power dc power supply at repetition rates up to 60 kHz. Modulation is performed by a series and shunt switch, each made up of a large array of power MOSFET devices. Redundant fault protection, including a novel technique for implementing a saturable reactor as a fault current limiter, is provided to ensure system survival during the many load short circuit faults expected in normal operation.

The operation of this pulsed power supply has met or exceeded all of the critical design goals, including switched voltage, peak current, RMS current, average current, and rep-rate. Since many of the design parameters are conservatively rated, extension of these performance levels to higher values should be possible. For example, the FET switch arrays have been operated at frequencies of up to 100 kHz during prototype testing. The primary limitation to extending the rep-rate capability at this time is the resistor in series with the shunt switch array, which has been sized for operation at lower frequencies. As long as the maximum device limitations are not exceeded and if slightly reduced reliability is acceptable, this system should be capable of operating at higher power levels and repetition rates.

References

[1] G.T. Santamaria and R.M. Ness, "High Power Switching Using Power FET Arrays", Sixth IEEE Pulsed Power Conference, Arlington, VA, 1987, pp. 161-164.